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FAKULTÄT FÜR TECHNISCHE WISSENSCHAFTEN

2

Hardware-Software Co-Simulation Environment for a Multiplier Free Blocker Detection Approach for LTE Systems



# Outline

- Introduction
  - Analog and digital front ends of the user equipment
  - Blocker environment worst case and relaxed
  - Power on demand receiver
- Co-simulation verification environment efficient hardware implementation
  - Co-simulation verification principle
  - Hardware testbed
- Conclusion and future work



## Introduction – Main Idea

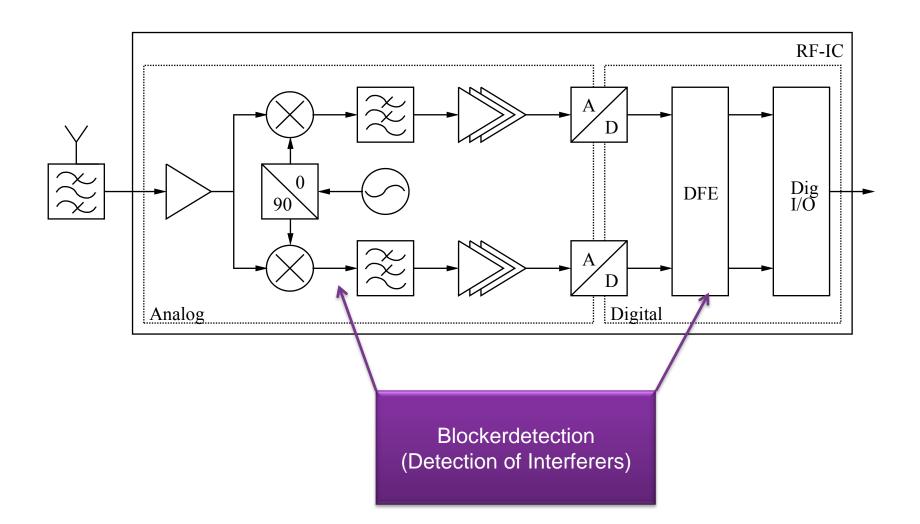
- Problem
- LTE UEs waste energy
- Reason
- Analog and digital front ends are over engineered as per the worst case 3GPP LTE standards
- Possible solution
  - Relaxing the front ends when the spectral environment is not so bad
  - Therefore it saves energy
- Possible approach
  - Reconfiguring the front ends by sensing the actual spectral environment
  - Using low complex filter bank based on a dyadic structure

4

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### Frontends of a UE

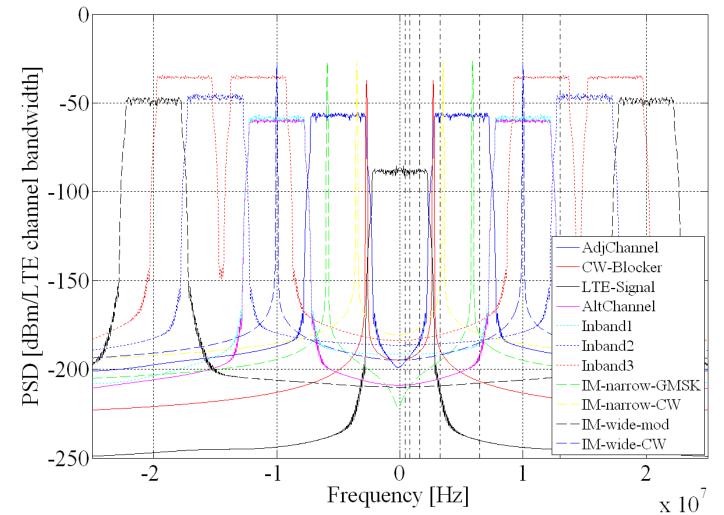




#### Worst case scenario according to 3GPP standard

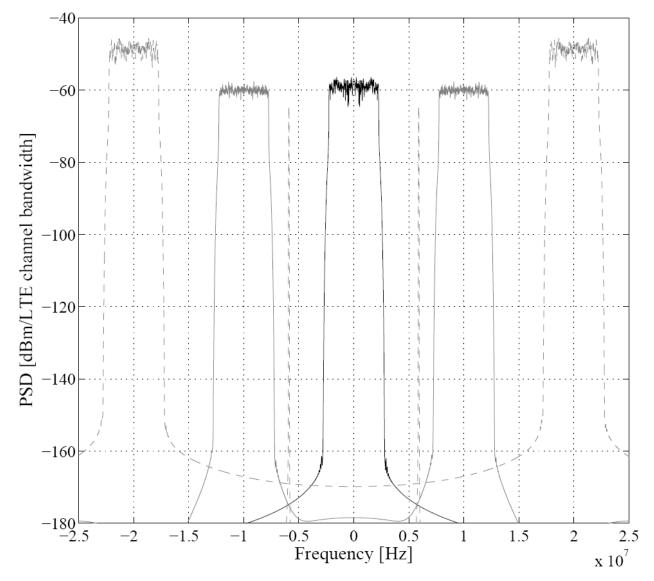
5

PSD: blocker overview





#### Relaxed blocker environment





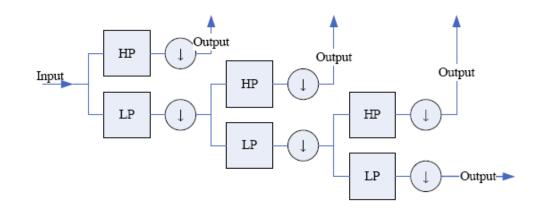
#### Power on demand receiver

- Full performance mode (worst case)
  - Highly linear amplifiers
  - Filters with steep slopes
  - High dynamic range for ADCs
  - Leading to high power consumption
- Relaxed mode (typical case)
  - The performance of the receiver relaxed
  - Leading to saving in energy



#### Desired: Blocker Detection Unit

- Blocker Detection Unit with (desired)
  - minimum complexity (computationally -> power consumption)
  - minimum cost (chip area)
  - maximum blocker detection accuracy
- Chosen approach
  - filter bank based spectrum sensing chain
  - Based on dyadic filter

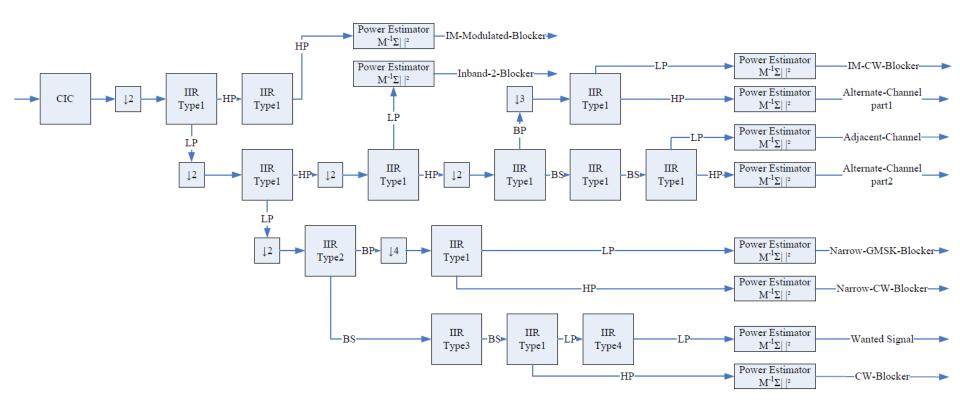


9

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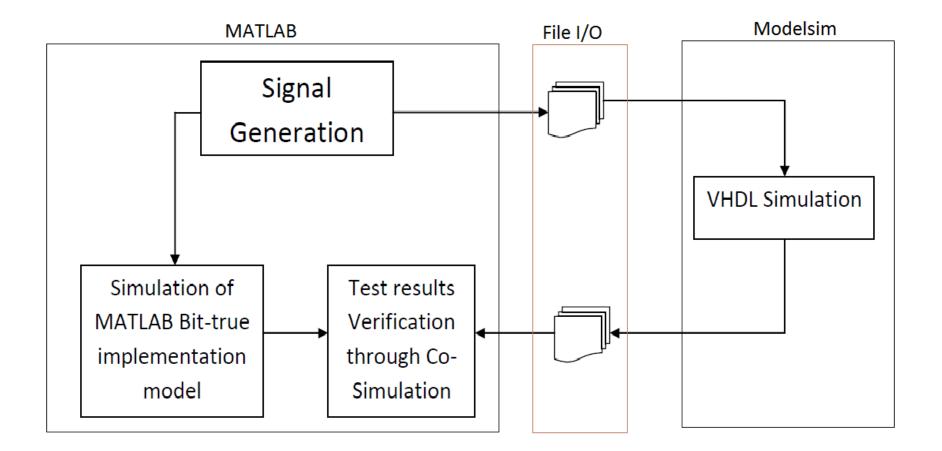


## Example chain for 20MHz testcase

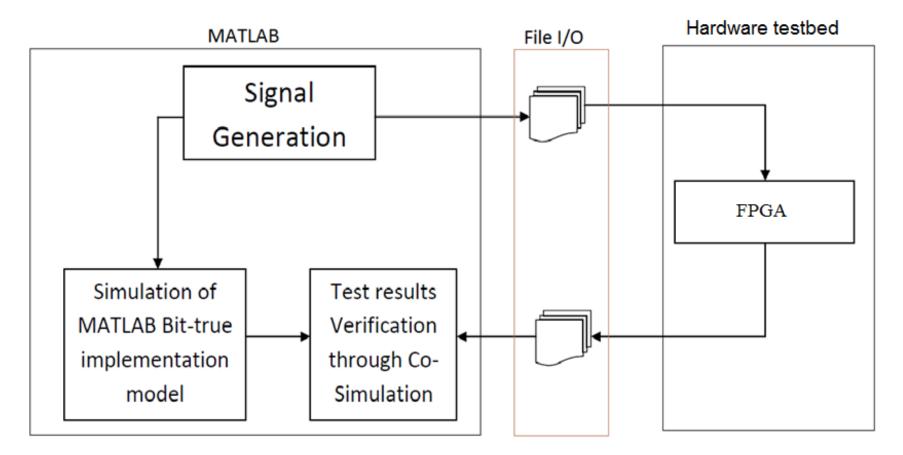




### **Co-Simulation Verification Principle**



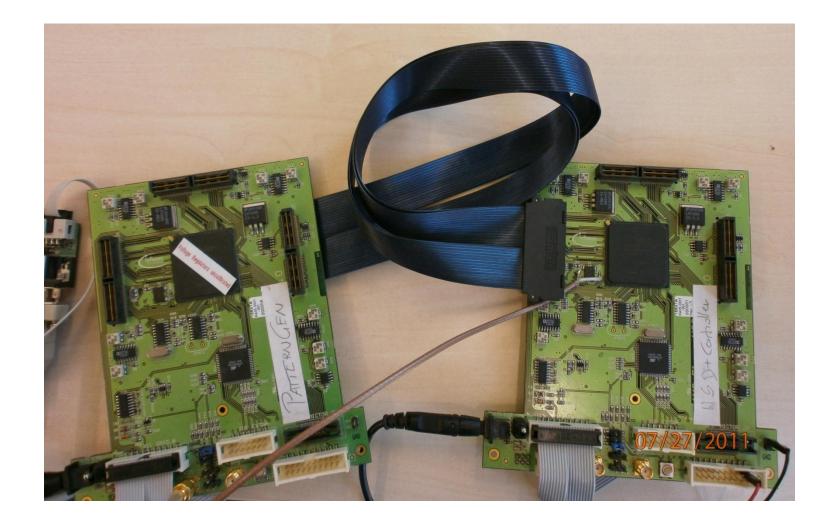
#### Hardware-Software Co-Simulation Verification Principle



11



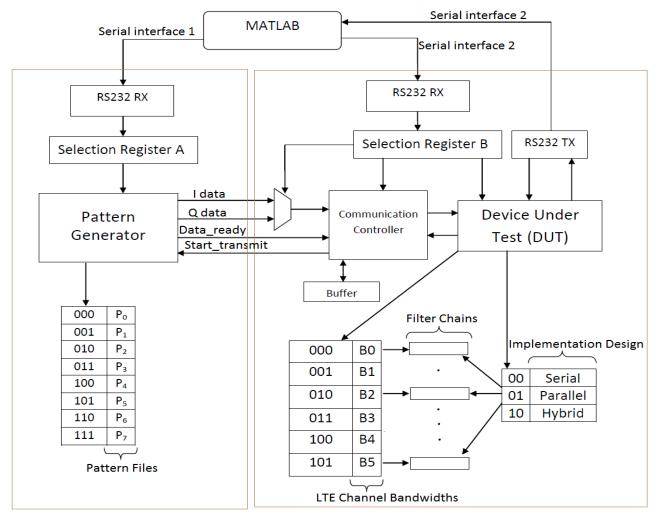
#### Hardware set-up used



13



#### Hardware test bed for the verifcation



Xilinx FPGA Board 2



# Conclusion

14

- Hardware-Software co-simulation environment presented
- Used for the verification of the multiplier free blocker detection approach for LTE sytems
- Efficient evaluation of the blocker detection unit is made possible
- Future work
  - Complexity estimation
  - Power consumption estimation
  - Prototype test on a test chip

# Thank you!

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